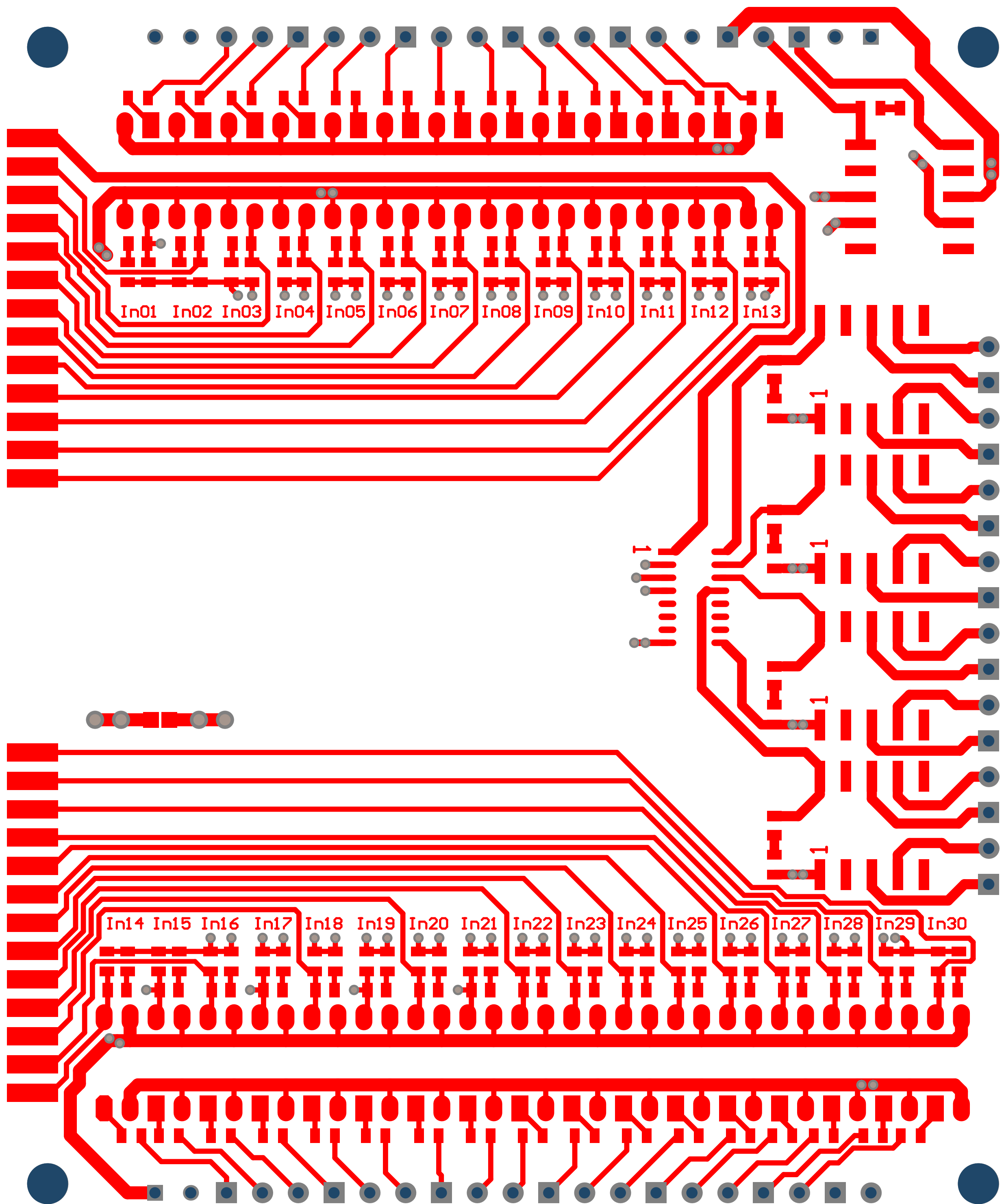
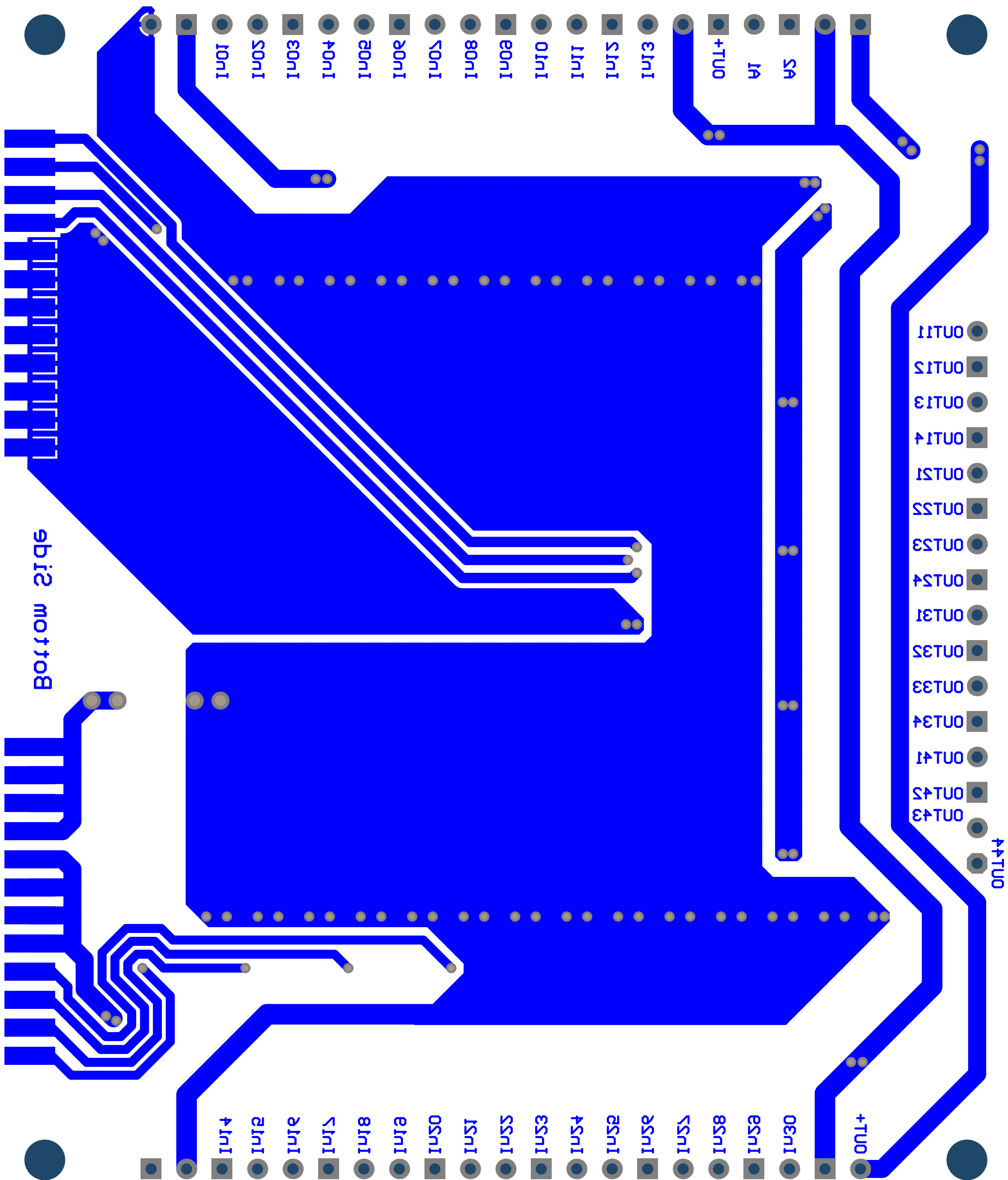
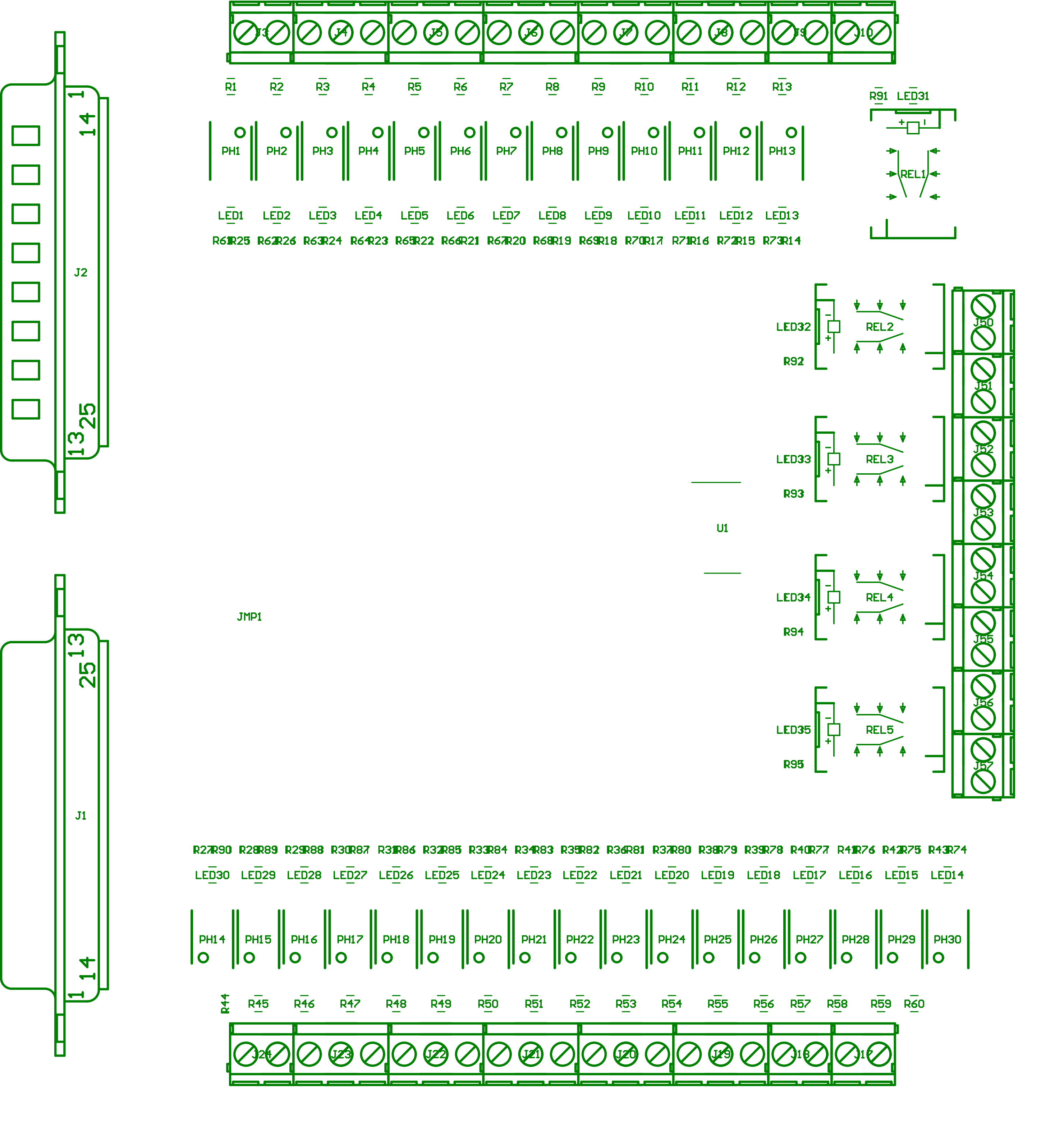
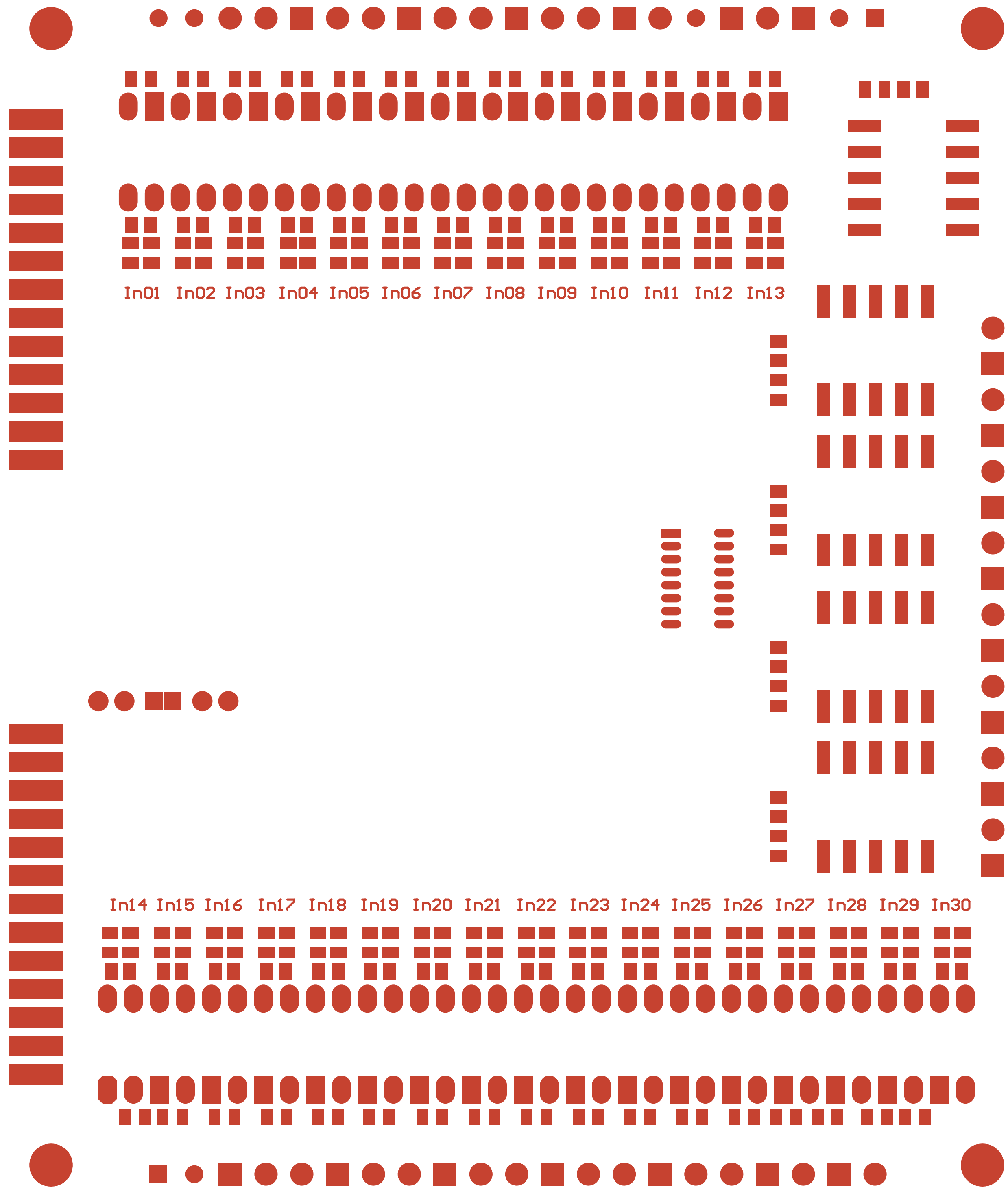


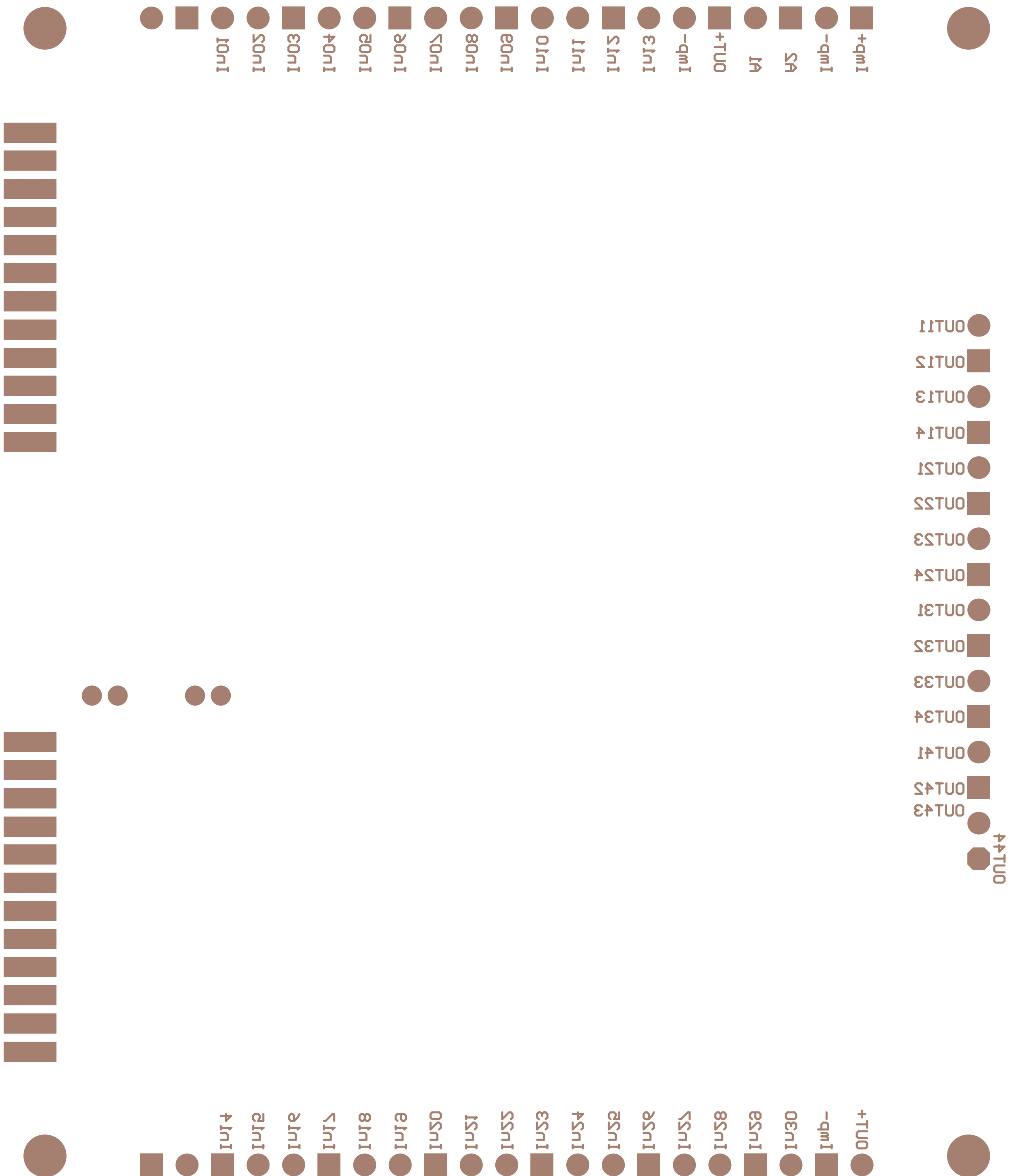
Title		
Size	Number	Revision
A3		
Date:	25.1.2016 r.	Sheet of
File:	D:\PCB\Customers\DIVDIV\LPT\LPT.Sch	Drawn By:

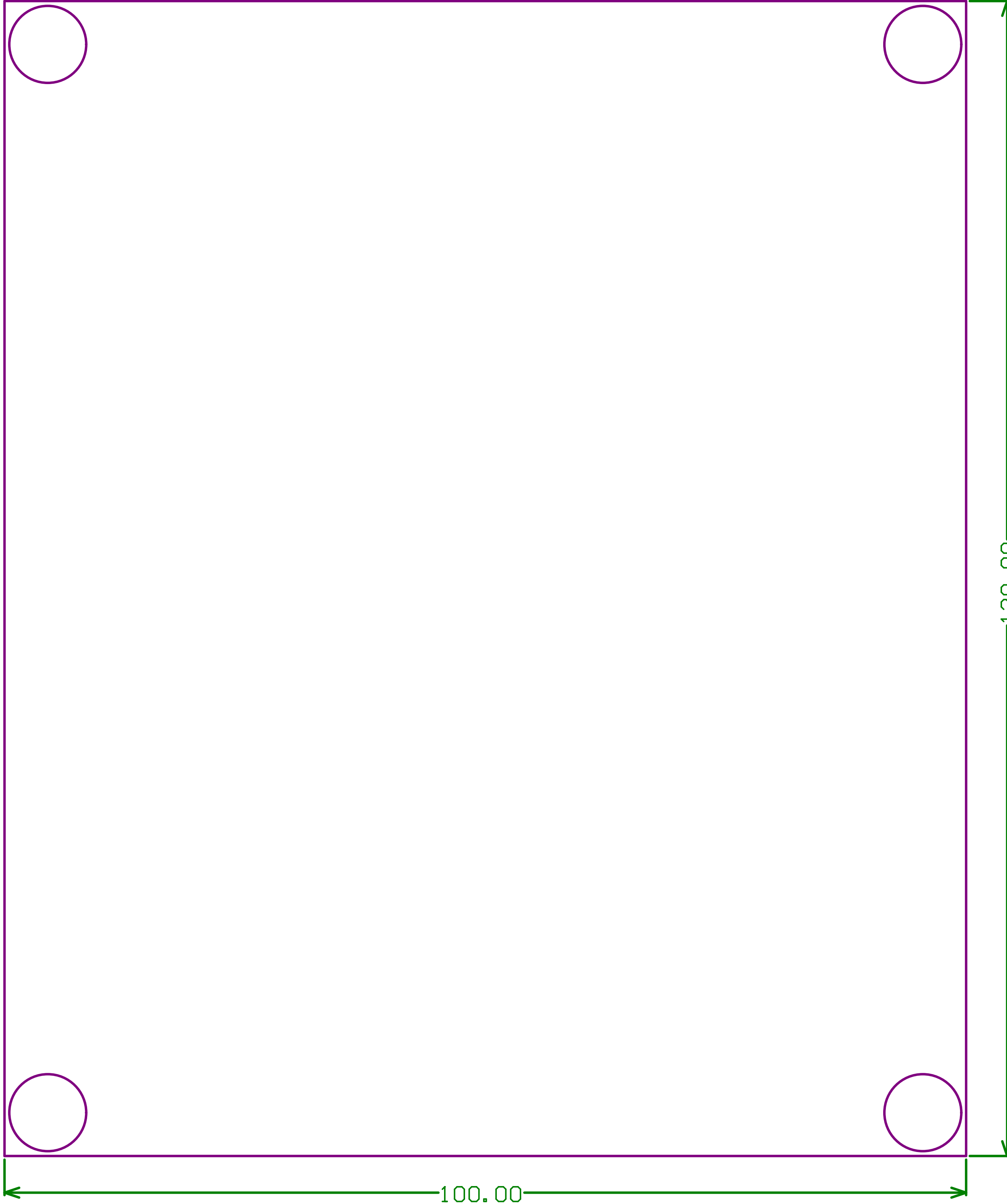


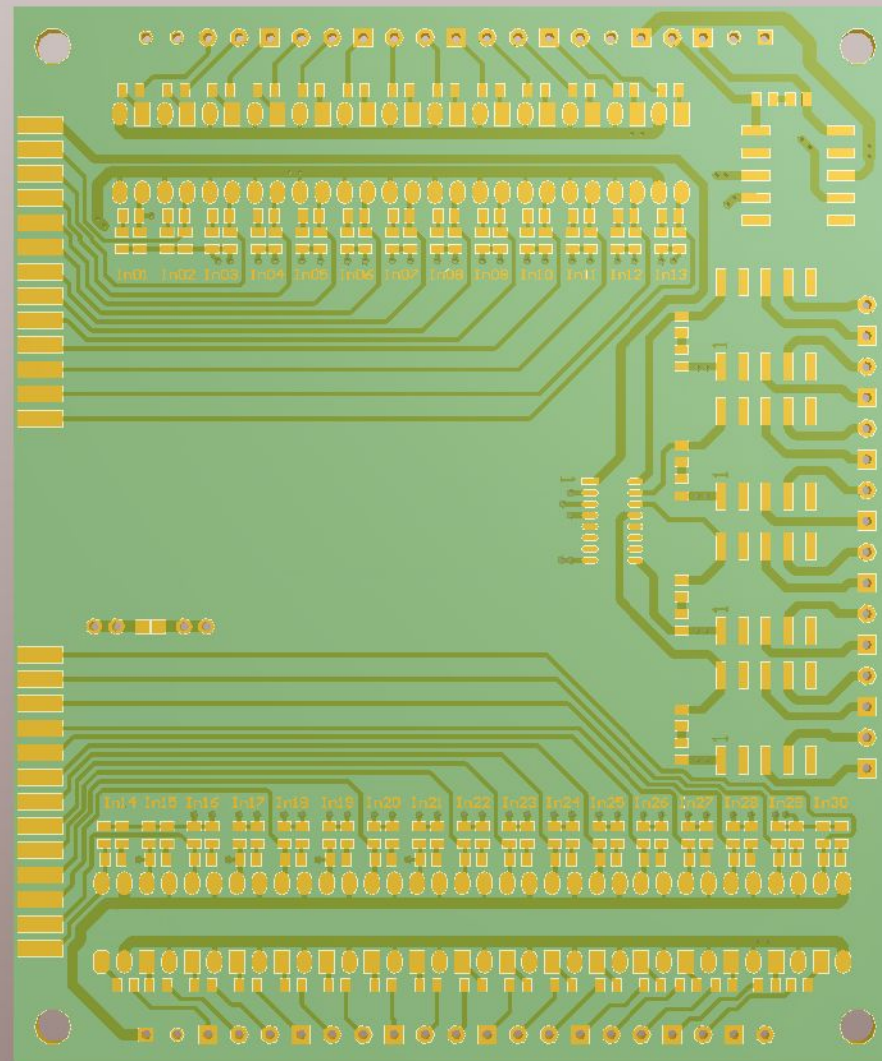


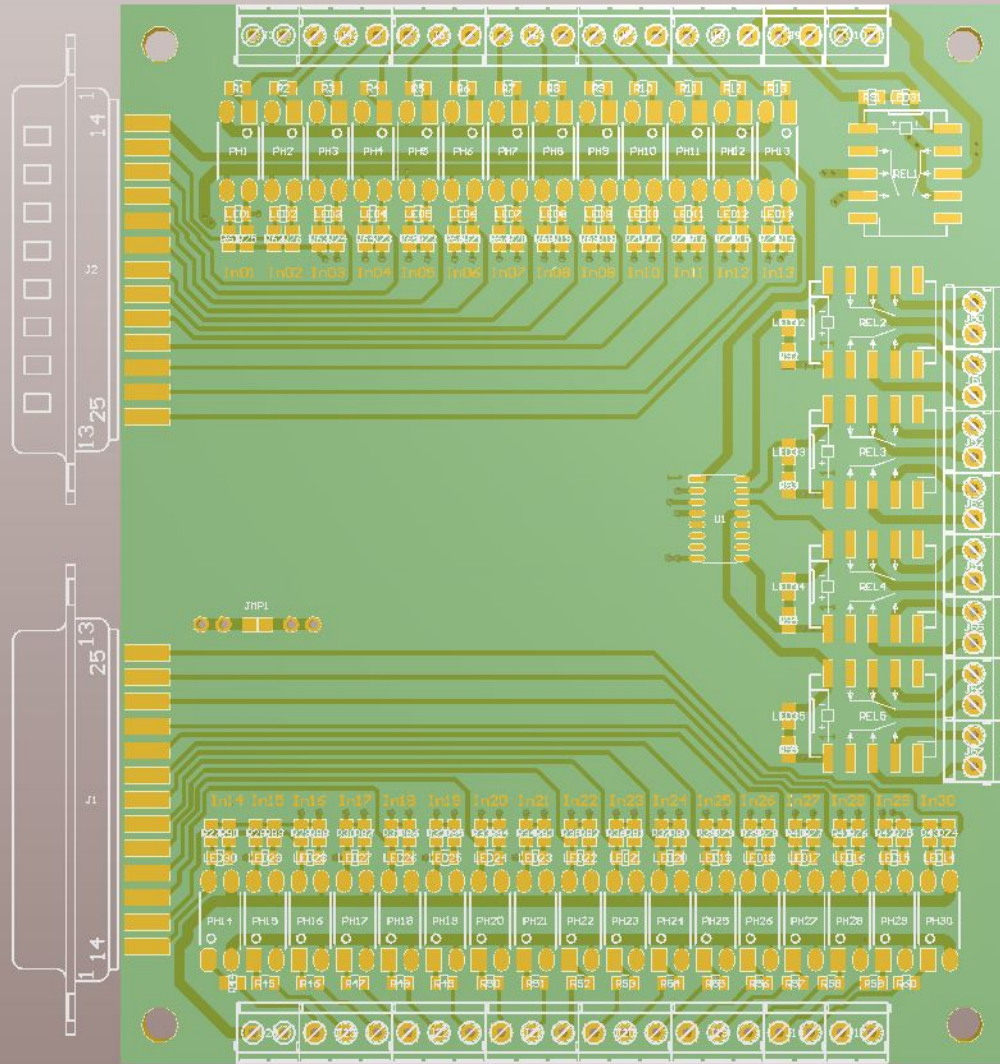


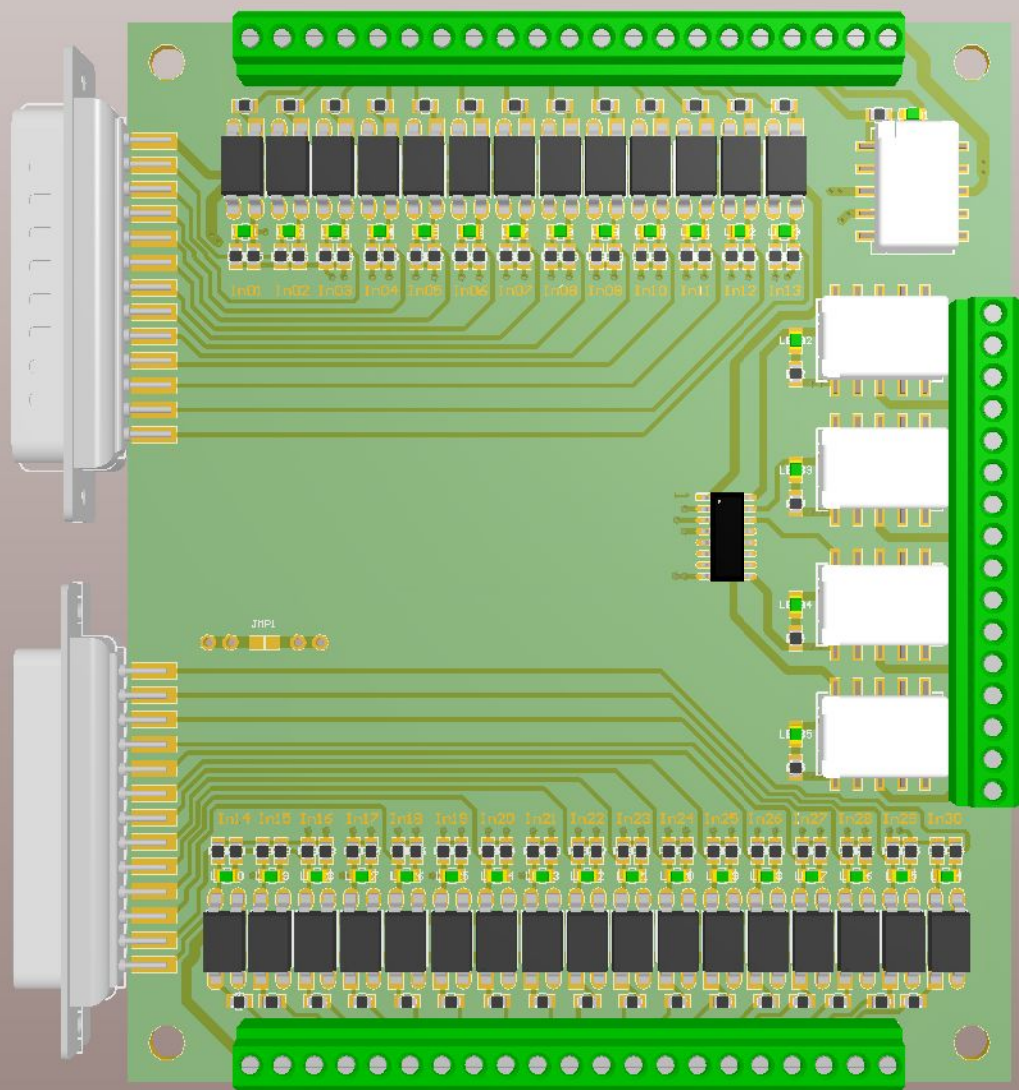


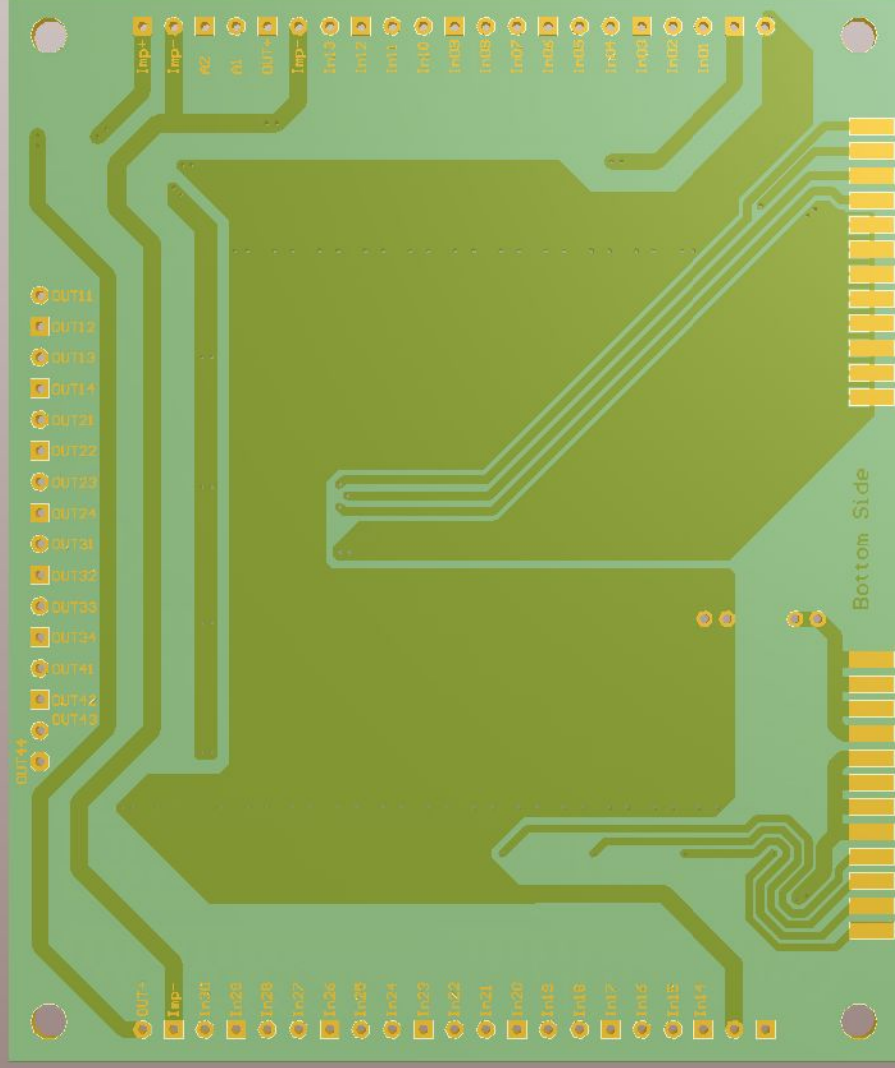


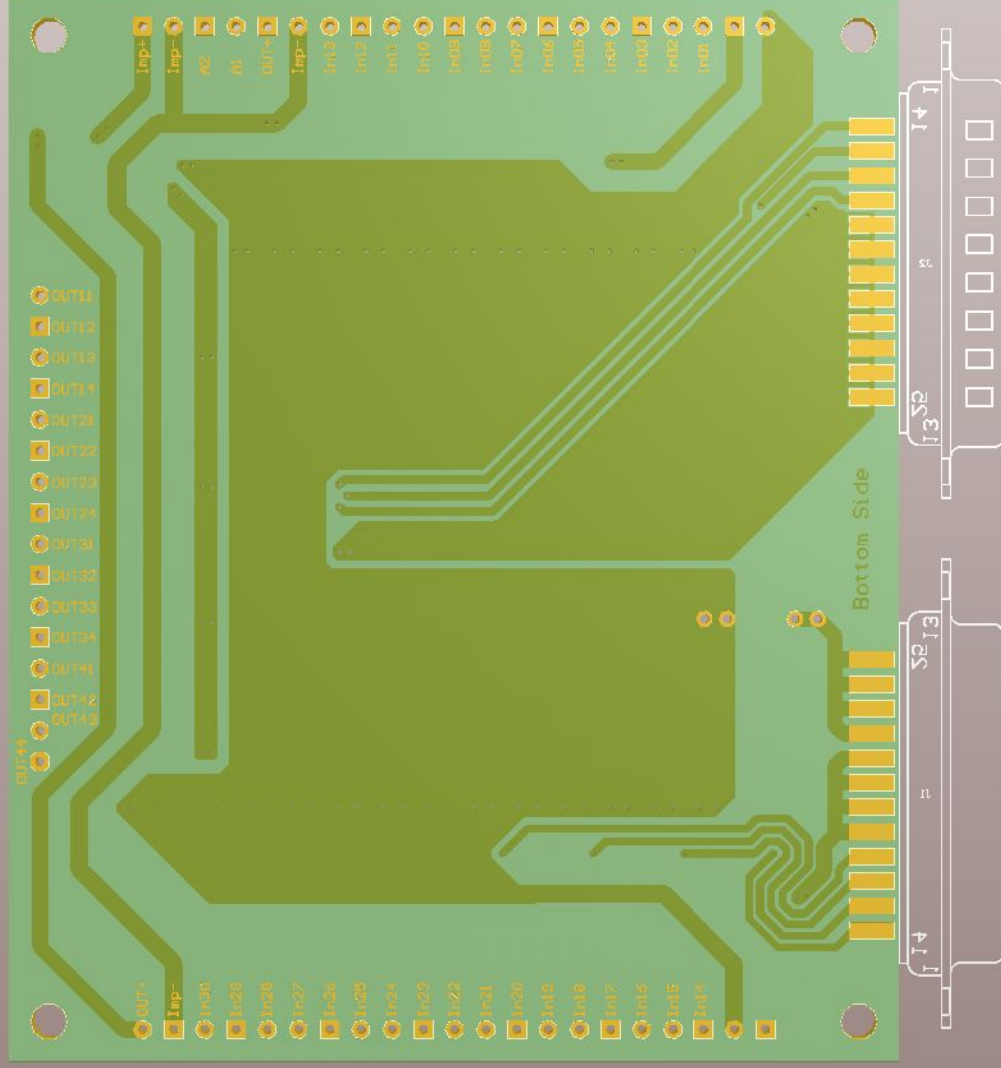


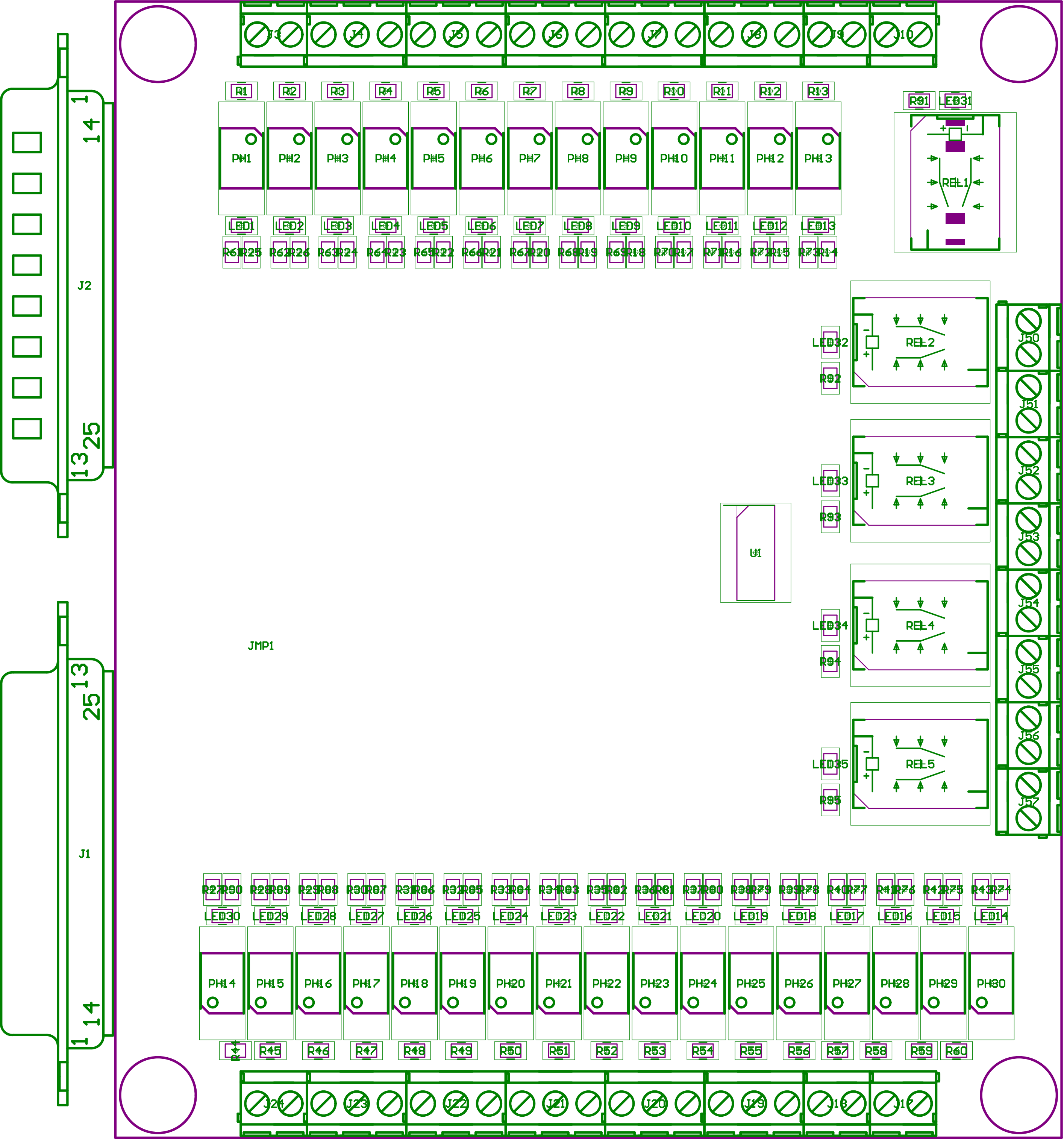




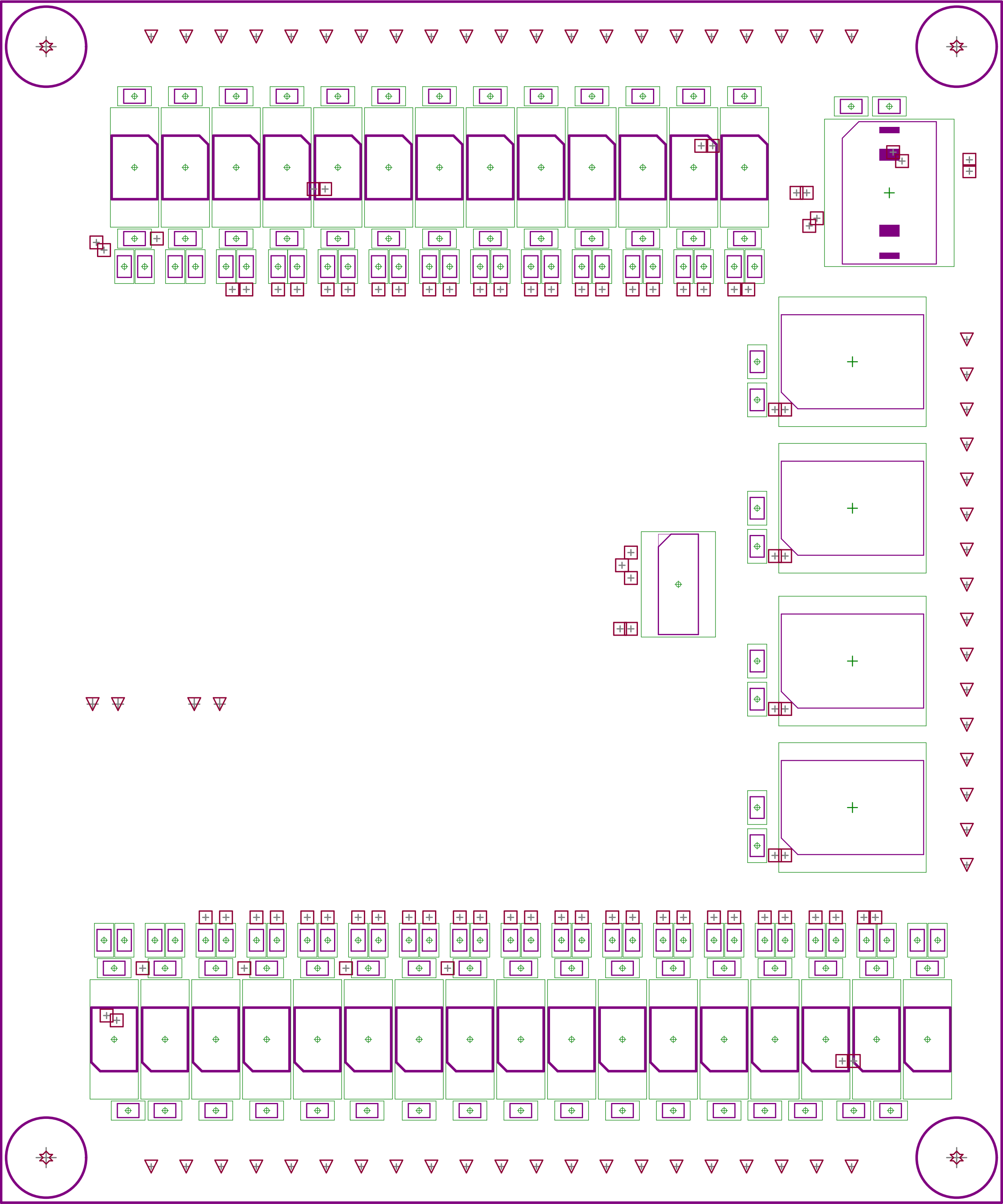












Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Technology
□	86	0.600mm (23.62mil)	PTH	Round	Top Layer - Bottom Layer	Via	Rounded	v102h60m0mx0
▽	62	1.100mm (43.31mil)	PTH	Round	Top Layer - Bottom Layer	(Mixed)	(Mixed)	(Mixed)
☆	4	4.000mm (157.48mil)	PTH	Round	Top Layer - Bottom Layer	Pad	Rounded	c400h400
	152 Total							

Design Rules Verification Report

Filename : D:\PCB\Customers\DIVDIV\LPT\LPT.PcbDoc

Warnings 0
Rule Violations 0

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=0.051mm) (Is Text),(All)	0
Clearance Constraint (Gap=0.508mm) (InPoly),(All)	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Net Antennae (Tolerance=0mm) (All)	0
Silk primitive without silk layer	0
Silk to Silk (Clearance=0.254mm) (Disabled)(All),(All)	0
Silk To Solder Mask (Clearance=0.254mm) (Disabled)(IsPad),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (Disabled)(All),(All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Hole Size Constraint (Min=0.025mm) (Max=25.4mm) (All)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Width Constraint (Min=0.254mm) (Max=25.4mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor	0
Width=0.254mm)	0
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Total	0