5I22
ANYTHING I/O
MANUAL

1.5

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GENERAL

DESCRIPTION

The MESA 5I22 is a general purpose programmable I/O card for the PCI bus. The 5I22 uses a 1M or 1.5M gate Xilinx Spartan3 FPGA for all logic, so it is truly an "Anything I/O" card. The FPGA is downloadable from the PCI bus side, allowing creation of almost any kind of specialized I/O function, even including multiple 32 bit processors in the FPGA.

Several pre-made functions are provided, including a 96 bit parallel I/O card with four 24 bit ports, a 16 channel host based servo motor controller, a 8 channel micro-controller based servo motor controller (*Soft*DMC), and a 16 channel, 32 bit timer counter card capable of running at 100 MHz. VHDL source is provided for all examples.

A bus mastering PCI bridge is used to support high bandwidth I/O. 10 LVDS pairs are available on one I/O connector for high speed card-card interfaces.

HARDWARE CONFIGURATION

GENERAL

Hardware setup jumper positions assume that the 5I22 card is oriented in an upright position, that is, with the PCI connector facing the user, and the white PCB markings right side up.

DEFAULT SETUP

EEPROM ENABLED

P3 VCCIO = 3.3V

CONNECTOR POWER = 5V (ALL)

PULLUP POWER = 3.3V

BUS SWITCH MODE = 3.3V

These default jumper positions are shown in the default jumper position picture on page 5.

EEPROM ENABLE

The PLX9054 PCI-Local bus bridge chip is configured at power up via a serial EEPROM. If the EEPROM is somehow mis-programmed or corrupted, it can be impossible to re-write the EEPROM from the PCI bus. To avoid this problem, The EEPROM can be temporarily disabled. W14 controls the EEPROM enable function, When W14 is in the up position (default) the EEPROM is enabled. When W14 is in the down position, the EEPROM is disabled. To fix a broken EEPROM setup, you must power up the 5I22 card with the EEPROM disabled, Enable the EEPROM, and re-write the EEPROM.

CONNECTOR POWER

The power connection on the I/O connectors pin 49 can supply either 3.3V or 5V power. Supplied power should be limited to 400 mA per connector.

When the following jumpers are in the up position, 5V power is supplied to pin 49 of the associated connector. When the jumper is in the down position, 3.3V power is supplied to to pin 49 of the associated connector.

W1 selects the voltage supplied to P2. (I/O connector for bits 0..23)

W4 selects the voltage supplied to P3. (I/O connector for bits 24..47)

W7 selects the voltage supplied to P4. (I/O connector for bits 48..71)

W10 selects the voltage supplied to P5. (I/O connector for bits 72..95)

HARDWARE CONFIGURATION

PULLUP POWER

Pullup resistors are provided for all I/O pins, These pullups can simplify interfacing to open collector devices such as mechanical switches, OPTO isolators and OPTO interrupters. Pullup voltage can be selected to be 5V or 3.3V on a per connector basis. When the pullup voltage jumper is in the 'up' position, 5V pullup voltage is selected, when the jumper is in the 'down' position, 3.3V pullup voltage is selected.

W2 selects the pullup resistor voltage for P2

W5 selects the pullup resistor voltage for P3

W8 selects the pullup resistor voltage for P4

W11 selects the pullup resistor voltage for P5

BUS SWITCH MODE

The 5I22 uses bus switch devices in series with all I/O pins. These devices allow the 5I22 inputs to be 5V tolerant and allow the I/O pins to be pulled up to 5V. The bus switch input protection function works by disconnecting the FPGA from the IO pins when the IO pin voltage rises above a preset threshold. This threshold determines the bus switch operational mode and is selectable on a per connector basis. We refer to the modes as 5V mode and 3.3V mode.

When in 5V mode, the inputs and tri-stated outputs may be pulled up to 5V. This allows driving 5V referred loads such as I/O module racks. The disadvantage of 5V mode is that the output impedance is higher in the high output state (when the FPGA pins are at 3.3V) as the bus switch is off when the FPGA pin is at 3.3V.

When 3.3V mode is selected, the bus switch is always fully on unless input voltages >4V are applied, at which point the bus switch disconnects the FPGA from the I/O pin. 3.3V mode is suggested for general use.

When the bus switch mode jumper is in the 'up' position, 5V mode is selected, when 'down', 3.3V bus switch mode is selected.

W3 Sets bus switch mode for P2, IO 0..23

W6 Sets bus switch mode for P3, IO 24..47

W9 Sets bus switch mode for P4, IO 48..71

W12 Sets bus switch mode for P5, IO 72..95

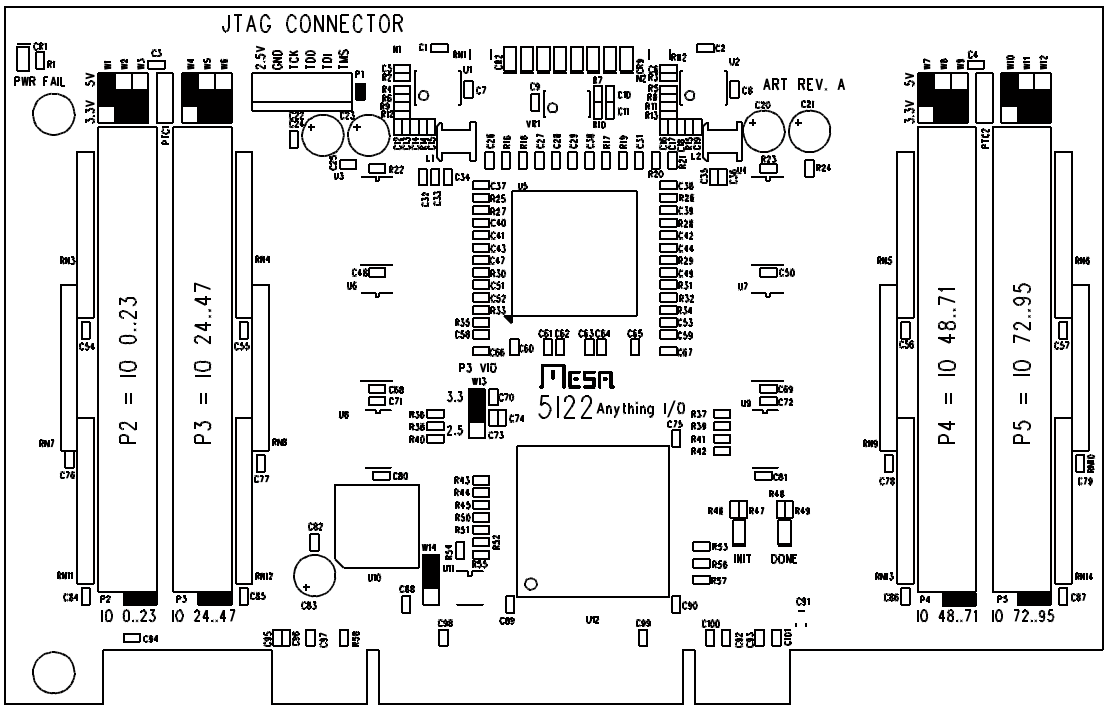
HARDWARE CONFIGURATION

P3 VCCIO

The IO bank that connects to P3 can have 3.3V or 2.5V power. This is intended to allow LVDS operation on connector P3. Jumper W13 selects the IOVCC for this bank. When W13 is in the up position, 3.3V IOVCC is selected for the bank connected to P3. When W13 is in the down position, 2.5V is selected for the bank connected to P3.

CONNECTORS

CONNECTOR LOCATIONS AND DEFAULT JUMPER POSITIONS



CONNECTORS

I/O CONNECTORS

P2, P3, P4 and P5 are the 5I22s I/O connectors. These are 50 pin box headers that mate with standard 50 conductor female IDC connectors. Suggested mating connector is AMP PN 1-1658621-0. For information on which I/O pin connects to which FPGA pin, please see the 5I22IO.PIN file on the 5I22 distribution disk. 5I22 IO connector pinouts are as follows:

P2 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	IO0	2	GND	3	IO1	4	GND
5	IO2	6	GND	7	IO3	8	GND
9	IO4	10	GND	11	IO5	12	GND
13	IO6	14	GND	15	IO7	16	GND
17	IO8	18	GND	19	IO9	20	GND
21	IO10	22	GND	23	IO11	24	GND
25	IO12	26	GND	27	IO13	28	GND
29	IO14	30	GND	31	IO15	32	GND
33	IO16	34	GND	35	IO17	36	GND
37	IO18	38	GND	39	IO19	40	GND
41	IO20	42	GND	43	IO21	44	GND
45	IO22	46	GND	47	IO23	48	GND
49	POWER	50	GND				

CONNECTORS

I/O CONNECTORS

P3 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	IO24/D0N	2	GND	3	IO25/D0P	4	GND
5	IO26/D1N	6	GND	7	IO27/D1P	8	GND
9	IO28/D2N	10	GND	11	IO29/D2P	12	GND
13	IO30/D3N	14	GND	15	IO31/D3P	16	GND
17	IO32/D4N	18	GND	19	IO33/D4P	20	GND
21	IO34/D5N	22	GND	23	IO35/D5P	24	GND
25	IO36/D6N	26	GND	27	IO37/D6P	28	GND
29	IO38/D7N	30	GND	31	IO39/D7P	32	GND
33	IO40/D8N	34	GND	35	IO41/D8P	36	GND
37	IO42/D9N/C	38	GND	39	IO43/D9P/C	40	GND
41	IO44	42	GND	43	IO45	44	GND
45	IO46	46	GND	47	IO47	48	GND
49	POWER	50	GND				

DIFFERENTIAL PAIRS

The 5I22 supports LVDS signaling on 10 pairs of the P3 I/O connector. The pairs are marked DNx and DPx in the table above. These signals are connected to the FPGA with 100 ohm impedance differential traces on the 5I22 PCB. Note that when LVDS is used, P3's VCCIO must be set to 2.5V. All pairs are length matched so the the PCB delays add less than 50 pS to the pair-pair skew.

CONNECTORS

I/O CONNECTORS

P4 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	IO48/CLK3	2	GND	3	IO49	4	GND
5	IO50	6	GND	7	IO51	8	GND
9	IO52	10	GND	11	IO53	12	GND
13	IO54	14	GND	15	IO55	16	GND
17	IO56	18	GND	19	IO57	20	GND
21	IO58	22	GND	23	IO59	24	GND
25	IO60	26	GND	27	IO61	28	GND
29	IO62	30	GND	31	IO63	32	GND
33	IO64	34	GND	35	IO65	36	GND
37	IO66	38	GND	39	IO67	40	GND
41	IO68	42	GND	43	IO69	44	GND
45	IO70	46	GND	47	IO71	48	GND
49	POWER	50	GND				

CONNECTORS

I/O CONNECTORS

P5 CONNECTOR PINOUT

PIN	FUNC	PIN	FUNC	PIN	FUNC	PIN	FUNC
1	IO72/CLK2	2	GND	3	IO73	4	GND
5	IO74	6	GND	7	IO75	8	GND
9	IO76	10	GND	11	IO77	12	GND
13	IO78	14	GND	15	IO79	16	GND
17	IO80	18	GND	19	IO81	20	GND
21	IO82	22	GND	23	IO83	24	GND
25	IO84	26	GND	27	IO85	28	GND
29	IO86	30	GND	31	IO87	32	GND
33	IO88	34	GND	35	IO89	36	GND
37	IO90	38	GND	39	IO91	40	GND
41	IO92	42	GND	43	IO93	44	GND
45	IO94	46	GND	47	IO95	48	GND
49	POWER	50	GND				

OPERATION

FPGA

The 5I22 use a Xilinx Spartan-III 1M or 1.5M gate FPGA in a 320 BALL BGA package: XC3S1000-FG320 or XC3S1500-FG320.

FPGA PINOUT

The local bus and I/O interface FPGA pinouts are described in the 5I22INFC.PIN and 5I22IO.PIN files in CONFIGS directory of the distribution disk. The 5I22IO.PIN file may be used as a template for custom configurations.

MEMORY AND I/O REGIONS

The PLX9054 PCI bridge local configuration registers can be accessed via I/O or memory. These are used to setup the PCI bridge, and for manipulating the I/O bits when configuring the FPGA.

BAR	MEM - I/O	WIDTH	RANGE
BAR 0	MEMORY	32 BITS	128 BYTES
BAR 1	I/O	32 BITS	128 BYTES

The PLX9054 PCI bridge allows for 2 separate memory and I/O regions to be mapped to the local bus that connects to the FPGA. The default EEPROM configuration sets these up as follows:

BAR	ADDRESS SPACE	MEM - I/O	WIDTH	RANGE
BAR 2	0	I/O	32 BITS	256 BYTES
BAR 3	1	MEMORY	32 BITS	64K BYTES

LOCAL BUS INTERFACE

The 5I22 uses the multiplexed local bus option of the PLX9054 bridge chip to save FPGA pins. Because of this multiplexed bus, the FPGA interface logic must latch the LAD bus when ADS is active to create an internal address.

OPERATION

CONFIGURATION

Before the 5I22 can do anything useful it must have its FPGA configuration data downloaded from the host CPU to the FPGA on the 5I22. This is done by writing a series of bytes from the configuration file to the 5I22 card's configuration data register. Configuration data is written a byte at a time (Right justified) to any of the I/O or memory bus space regions mapped to the 5I22s local bus.

The FPGA configuration control bits must be manipulated before configuration data can be sent to the FPGA. These control bits are controlled via GPIO pins of the PLX9054 PCI bridge. The PLX9054s GPIO pins are connected to the following FPGA configuration pins:

GPIO	DIRECTION	FPGA	ALTERNATE
GPI	IN	DONE	/DACK
GPO	OUT	/PROGRAM	/DREQ

Note that the DONE and /PROGRAM bits are multiplexed with DMA control lines. If these DMA control lines are needed, the DISABLECONF pin on the FPGA needs to be asserted or a /DREQ signal will reset the FPGA

SC5I22

A DOS utility program SC5I22.EXE is provided to send configuration files to the 5I22. The Pascal and C source for this program is available on the distribution disk, and can be used as an example for writing a custom version of download software. SC5I22 is invoked with the FPGA configuration file and the 5I22 configuration base address on the command line:

```
SC5I22 FPGAFILE.BIN
```

SC5I22 uses binary FPGA configuration files. These files can be standard Xilinx BIT files or PROM format files. The SC5I22 utility sends PROM files directly to the 5I22. BIT files have their headers stripped and are bit reversed before being sent to the 5I22.

OPERATION

CONFIGURATION

SC9054W

Another utility SC9054W is provided for Windows 2000 and Windows XP This utility requires the PLX9054.SYS driver and PLXAPI.DLL API SHIM to work. The source for SC9054W can be used as an example of how to access the configured 5I22 cards under Windows 2K or XP.

SC9054W use binary FPGA configuration files. These files can be standard Xilinx BIT files or PROM format files. The SC9054W utility sends PROM files directly to the 5I22. BIT files have their headers stripped and are bit reversed before being sent to the 5I22.

OPERATION

CLOCK SIGNALS

The FPGA has one on card clock source and 4 available clock inputs. The on card clock is 48 MHz routed to GCLK5. This clock functions both as the FPGA system clock and the local bus interface clock. IOBITS 42 and 43 (connector P3) are FPGA GCLK7 and GCLK6 respectively. This pair of clocks can also be used as a single LVDS differential input clock. IOBIT 48 (connector P4) is GCLK3, and IOBIT 72 (connector P5) is GCLK2.

LEDS

The 5I22 has 8 FPGA driven user LEDs. The user LEDs can be used for any purpose, and can be helpful as a simple debugging feature. A low output signal from the FPGA lights the LED. See the 5I22IO.PIN file for FPGA pin locations of the LED signals.

IO LEVELS

The FPGA used on the 5I22 is a Spartan3. The Spartan3 supports many I/O standards. The 5I22 does not support use of the I/O standards that require input reference voltages, also VCCIO on the banks that connect to P2, P4 and P5 are fixed at 3.3V so only 5 I/O options can be used on P1 and P2. The available I/O options for P1 and P2 are LVTTL, LVCMOS_33, LVDCI_33, and LVDCI_33_DV2 . P3 can use a 2.5V VCCIO which adds the following I/O standards: LVCMOS_25, LVCMOS_25_DCI, LVDS_25, LVDS_25_DCI, LVDSEXT_25, LVDSEXT_25_DCI.

The Spartan3 FPGA chip used on the 5I22 is not 5V tolerant but external bus switch parts are used on the 5I22 to make the I/O pins 5V tolerant. The bus switch parts disconnect the FPGA pins from the I/O pins when the I/O pins are driven to positive voltage levels that would damage the FPGA.

The voltage level that causes disconnect can be selected to be ~4V (3.3V mode) or ~3.3V (5Vmode). For most applications, the 3.3V mode should be used. The 5V mode is useful when driving 5V referred loads.

Note that there is no protection against negative input voltages other than the input clamp diodes in the FPGA and bus switches, so negative input voltages must be limited to -.5V

STARTUP I/O VOLTAGE

After power-up or system reset and before the the FPGA is configured, the pull-up resistors will pull all I/O signals to a high level. If the FPGA is used for motion control or controlling devices that could present a hazard when enabled, external circuitry should be designed so that this initial state results in a safe condition.

OPERATION

TERMINATION

The FPGAs used on the 5I22 support series and parallel termination that can be programmed on a pin-for-pin basis. This feature is called DCI. The 5I22 supports DCI on all I/O pins. The DCI reference resistors are all 100 Ohm 1%.

POWER SUPPLY

The 5I22 uses on card switching regulators to supply the 3.3 VIO and 1.2V CORE core power for the FPGA. A linear low dropout regulator is used to supply the 2.5V VAUX and LVDS power The core power and 3.3V power supplies are rated at 3 Amp. The 2.5V power supply is limited to 500 mA. The 5I22 uses only the 5V power from the PCI bus.

SUPPLIED CONFIGURATIONS

IOPR24

The IOPR24 configuration creates a simple 72 bit parallel I/O port. IOPR24 is 32 bit device, all accesses read or write 32 bit words. IOPR24 creates three 24 bit ports, one port per I/O connector.. Each I/O bit can be individually programmed to be input or output. All I/O bits will be input on startup. For information on the register map of the IOPR24 configuration, see the regmap file in the /configs/IOPR24 directory of the 5I22 distribution disk.

5I22LOOP

The IOPR24 configuration provides a simple way to check that all the I/O pins are OK and that most of the host interface is working. A loopback program (5I22LOOP) is provided for doing this testing. 5I22LOOP depends on an external loopback cable between I/O connectors P2, P3, and P4. 5I22LOOP perform a rotating bit test with one I/O connector programmed as outputs and the other two as inputs. All combinations of inputs and outputs are tested. In addition, a 32 bit register readback test is performed to verify 32 bit local data bus functionality.

HOSTMOT2

The HOSTMOT2 configuration is a up to 16 channel host based servo motor or step motor controller. Host based controllers depend on the host CPU to "close" the servo loop. This has advantages and disadvantages. One advantage is that less hardware is needed, since host based software does all the math and handles all the control bits. Another advantage is that since the host based software is easily examined and modified, it is more amenable to customization and is more useful as a teaching tool. One disadvantage is that host based motor controllers depend on fast interrupt response time, since the control loop is an interrupt driven background task. This means that host based motor controllers don't tend to work well with multitasking operating systems such as Windows or Unix. They will work with real-time operating systems or simple operating systems like DOS.

SUPPLIED CONFIGURATIONS

HOSTMOT2

HOSTMOT2 is available in several configurations the vary the number of servo or step generator channels, plus miscellaneous I/O options including 32 bit buffered UARTs, SPI interfaces, SSI interfaces etc.

Demonstration software provided with the 5I22 implements a PID + feedforward control loop, plus a ramp-up, slew, ramp-down, profile generator for position control applications. Demo program (newmove.exe) and sources are located in the /configs/hostmot2/support directory of the 5I22 distribution disk..

*SOFT*DMC

The *Soft*DMC configuration creates a 4 or 8 axis processor based servo motor controller, with the processor embedded in the FPGA. The *Soft*DMC configuration has the advantage that the embedded processor takes care of all time critical functions, so it can control motor position and motions without host intervention.

The *Soft*DMC configuration has programmable sample and PWM rates, and can operate 4 axis at up to 50 KHz sample rate and 8 axis at up to 25 KHz sample rate.

The control loop is a PID+F loop (F=feedforward) with 16 bit tuning parameters. Position and Velocity use 32 bit parameters for wide range.

The profile generator supports position,velocity, and homing modes. Position mode includes ramp-up, slew, ramp-down motions. Velocity mode supports breakpoints and a linked list parameter loading system for accurate profiling. Profile generator uses 48 bit accumulator to allow velocities from 2 turns per day (500 line - 2000 count encoder, 4 KHz sample rate) to 60,000 RPM.

There is a separate manual available for the *Soft*DMC motion controller.

Demo programs, and tuning program (dmctune.exe) and sources are located in the /configs/softdmc/support directory of the 5I22 distribution disk.

REFERENCE

SPECIFICATIONS

POWER	**MIN**	**MAX**	**NOTES**:
POWER SUPPLY	4.5V	5.5V	
POWER CONSUMPTION:	----	2A	Depends on FPGA Configuration and external load
MAX 5V CURRENT TO I/O CONNS	---	400 mA	Per Connector
MAX 3.3V CURRENT TO I/O CONNS	---	400 mA	Per Connector
ABSOLUTE MAX I/O PIN VOLTAGE	-.5V	7V	
TEMPERATURE RANGE -C version	0 ^{o}C	+70 ^{o}C	
TEMPERATURE RANGE -I version	-40 ^{o}C	+85 ^{o}C	