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PCIE bus dual serial port and print port chip CH382

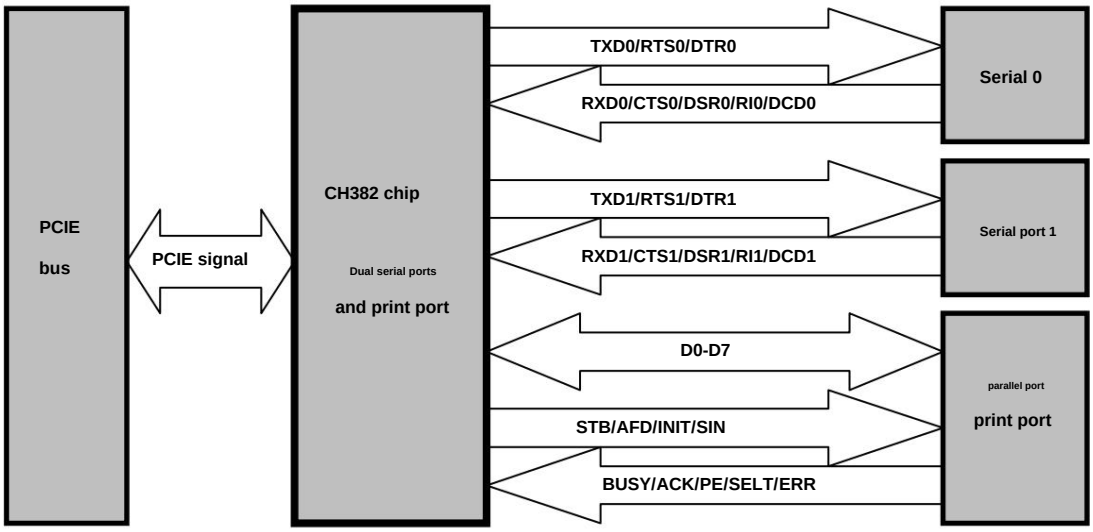
Introduction

Version: 1

http://wch.cn

1 Overview

CH382 is a dual serial port and print port chip for PCI-Express bus, including two asynchronous serial ports compatible with 16C550 or 16C750 port and one EPP/ECP enhanced bidirectional parallel port. Asynchronous serial port provides independent 256-byte FIFO buffer for sending and receiving, supporting up to 8Mbps It can be used for RS232 serial port expansion of PCIE bus, PCIE high-speed serial port with automatic hardware rate control, serial port Networking, RS485 communication, parallel port/print port expansion, etc. The figure below is a block diagram of its general application.



2. Features

2.1. Overview

- The same chip can be configured as dual serial ports, single parallel port/printing port, dual serial ports plus parallel port/printing port of PCIE bus.
- Provides a two-wire serial host interface, which can be connected to a serial EEPROM device similar to 24C0X for storing non-volatile data.
- The device identification (Vendor ID, Device ID, Class Code, etc.) of the PCIE board can be set in the EEPROM device.
- The driver supports Windows 98/ME/NT4.0/2000/XP/Vista/Win7/Server2003 and Linux.
- 3.3V power supply voltage, the main I/O pins support 5V withstand voltage, and the serial port low-power sleep mode is supported.
- The chip function is equivalent to CH367 chip plus CH438 chip, providing 4 serial ports, 8 serial ports and more serial port application solutions.
- Support PCMCIA ExpressCard notebook card.

2.2. Serial port

- Completely independent 2 asynchronous serial ports, compatible with 16C550, 16C552, 16C554 and 16C750 and enhanced.
- Supports 5, 6, 7 or 8 data bits and 1 or 2 stop bits.
- Support odd, even, no parity, blank 0, flag 1 and other parity methods.
- Programmable communication baud rate, support 115200bps and communication baud rate up to 8Mbps.
- Built-in 256-byte FIFO buffer, supporting 4 FIFO trigger levels.
- Support MODEM modem signal CTS, DSR, RI, DCD, DTR, RTS, which can be converted into RS232 level.
- Support hardware flow control signal CTS and RTS automatic handshake and automatic transmission rate control, compatible with TL16C550C.
- Support serial frame error detection and break line interval detection.
- Support full-duplex and half-duplex serial communication.

2.3. Parallel port

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- Support SPP, Nibble, Byte, PS/2, EPP, ECP and other IEEE1284 parallel/printing port working modes.
- Support bidirectional data transmission, support up to 1M bytes/second transmission speed.

3. Package

Package form	Body width	Pin pitch package description 15.7mil ultra-small		Order model
LQFP-64	7mm x 7mm	0.4mm	LQFP64 pin SMD CH382L	

4. Configuration

4.1. Global function configuration

CH382 chip has 3 functional modes:

MDPRT# pin	MDSEL pin	Function Mode/Device ID Abbreviation	
Connected to VCC33 or floating, that is = 1	Connected to VCC33 or floating, that is =1	Dual serial ports, DID=3253H	2S
Connect to GND, that is = 0	Connect to VCC33 or leave it in the air, that is = 1	Dual serial ports plus parallel port, DID=3250H	2S1P
connect to GND, that is = 0	Connect to GND, that is = 0	Single parallel port, DID=3050H	1P

The CKSEL pin of the CH382 chip is used to select the clock frequency of the internal 2 serial ports:

CKSEL is connected to VCC33 or left floating, that is, CKSEL=1, the clock is input from the XO pin, the frequency is determined by the external crystal, and the internal Part of the frequency coefficient defaults to 1/12 frequency division, and supports to select 2 times frequency through CK2X or CKnS;

CKSEL is connected to GND, that is, CKSEL=0, then input the clock from the XO pin, the frequency is determined by the external crystal, and the internal frequency coefficient It is always forced to be 2 times the frequency, for example, the serial port set to 115200bps by the application software is actually 230400bps;

If CKSEL is connected to the PERST# pin, that is, CKSEL=R, the internal crystal oscillator is disabled (the XI and XO pins can be left floating without External crystal and capacitor), and the clock with a frequency of 125MHz is provided by the internal PLL, and the internal frequency coefficient defaults to 1/68 frequency division, support to choose no frequency division through CK2X or CKnS. Obtained by dividing by 1/68 in the internal PLL mode The received 114.9Kbps is only 0.27% different from the standard 115.2Kbps, which is acceptable.

In single parallel port mode, CKSEL should be connected to the PERST# pin to disable the internal crystal oscillator.

4.2. External configuration chip

The CH382 chip will check the data in the external 24CXX configuration chip every time it is powered on or after the PCIE bus is reset.

If the configuration chip is configured and the data is valid, it will be automatically loaded into the CH382 chip to replace the default PCIE identification information.

The following table is the data definition in the configuration chip 24CXX.

Byte address abbreviation		Data usage	Defaults
00H	CFG	description External configuration chip valid flag, must be 52H	52H
01H	FREQ	bits 1 to 0 are used to select the internal frequency coefficient 0FFH of serial port 1 to serial port 0 (reserved	
03H-02H	RSVD	unit) Vendor ID: Vendor ID, the default is 1C00H Device ID: Device	0000H
05H-04H	VID	ID, referred to as DID Chip version: Revision ID Device class code: Class Code	customize
07H-06H	DID	Subsystem Vendor ID: Subsystem Vendor ID Subsystem ID: Subsystem ID	customize
08H	RID	(reserved unit) User or application custom unit	customize
0BH-09H	CLS		070005H
0DH-0CH	SVID		customize
0FH-0EH	SID		customize
1FH-10H	RSVD		00H or FFH
Other address APP			

5. Application

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5.1. Dual serial port + parallel port (below)

This is the basic circuit of PCIE dual serial port + parallel port/printing port based on CH382 chip, the RS232 level conversion chip is not included in the figure. U3 is an optional external configuration chip, and the online configuration tool software under Windows system is provided on the website.

IEEE1284 requires the print port signal to maintain impedance matching, so the print port parallel data line may require series resistance and parallel power. It can also be omitted when the requirements are not high.

Crystal X1 and capacitors C15 and C16 are used for the clock oscillator circuit. If the CKSEL pin is connected to the PERST# pin, then X1 and C15 and C16 can be omitted. Other capacitors are used for power decoupling. The capacitor with a capacity of 10uF is a tantalum capacitor, and the capacitor with a capacity of 0.1uF is a monolithic or high-frequency ceramic capacitor, which are respectively connected in parallel to the power pins of CH382.

CH382 supports common communication baud rates: 1200, 2400, 4800, 9600, 19.2K, 38.4K, 57.6K, 115.2K, 230.4K, 460.8K, 921.6K, 1.8432M, 2.7648M, 7.8125M, etc.

CH382 can be used to expand additional high-speed RS232 serial ports and parallel/printer ports for computers through PCIE bus, support automatic hardware high baud rate serial port, RS422 or RS485 communication interface, etc.

CH382 is a high frequency circuit, please refer to the PCIE bus specification when designing the PCB, or refer to the PCIE_PCB.PDF document.